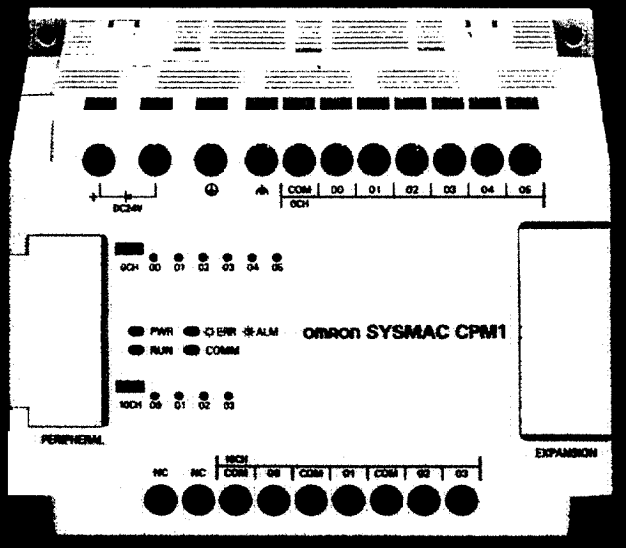
Programmable Controller

OMRON

SYSMAC

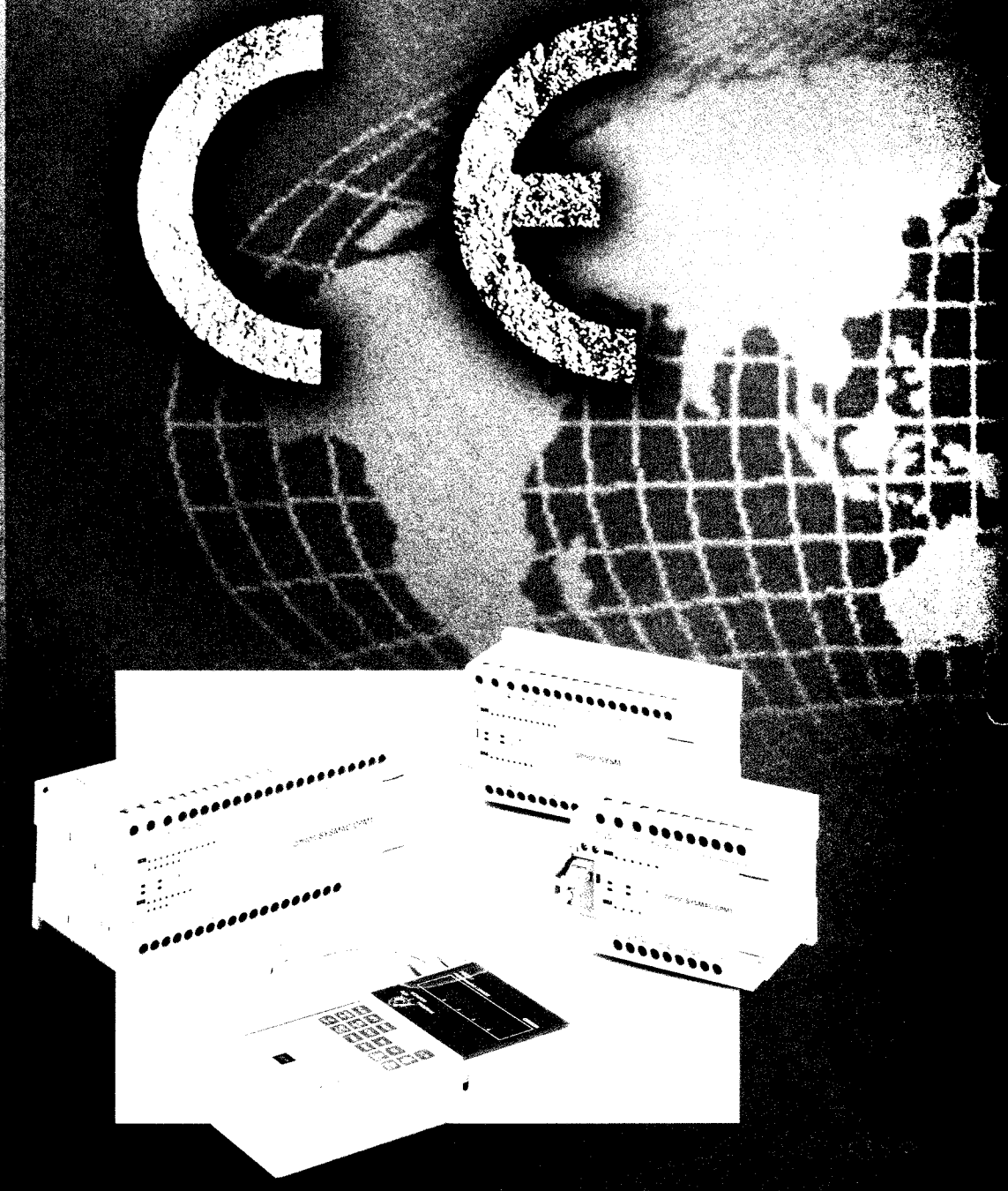
CPM1

The Safe Micro PLC



CPM1

The Powerful PLC Designed to Meet Global Standards at a Micro Price



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CPM1

The Safe, User-friendly, and Cost-effective Micro PLC

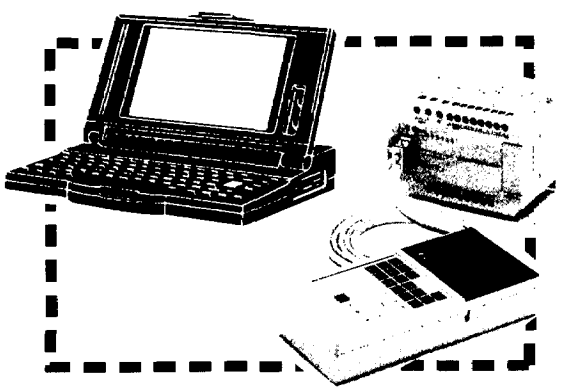
Conforms to EC Directives (EMC and Low Voltage) and Has the CE Marking

The CPM1 is well suited as part of equipment for use in the European market because it conforms with EC directives.

CE

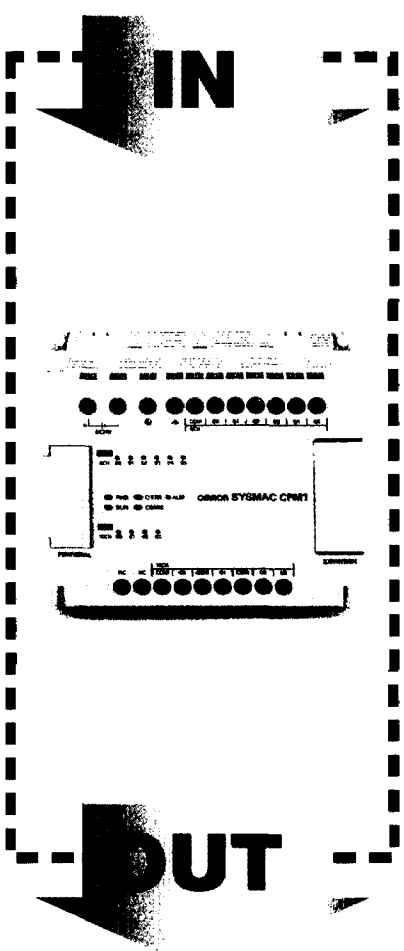
Same Programming Devices as Our Other Top-of-the-line Equipment

The CPM1 can be programmed using the Programming Console, SYSWIN, SYSMAC Support Software (SSS), and Laddder Support Software (LSS).



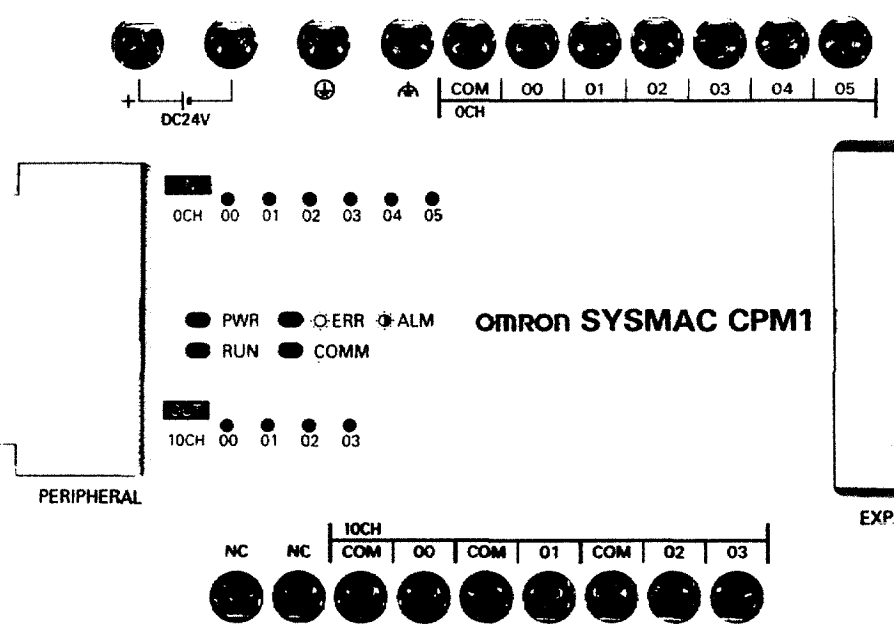
PLCs with Integrated I/O Terminals

The integrated PLCs are equipped with 10, 20, and 30 I/O terminals built right into the CPU. Moreover, a 20-point Expansion I/O Unit can be connected by cable to provide a maximum of 50 control points.



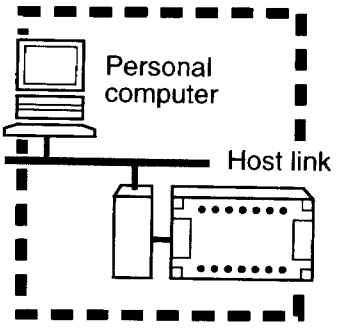
Offers Safety and Ease of Use.

10 points



Host Link Communications Available

Simply connect one of the optional adapters with the CPM1 PLC for RS-232C or RS-422 communications. The PLC can be connected to personal computers as well as other peripheral devices such as display terminals.



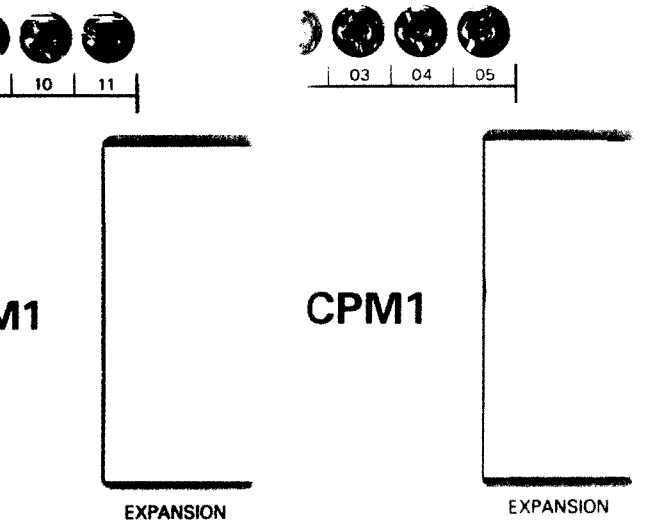
1:1 Link Compatibility

Data Areas can be linked by 1:1 connections between two CPM1 PLCs, one CPM1 PLC and one CQM1 PLC, or one CPM1 PLC and one C200HS PLC.

*An RS-232C Adapter is needed for the connection.

Offers Numerous Features in a Compact Size.

20 points **30 points**

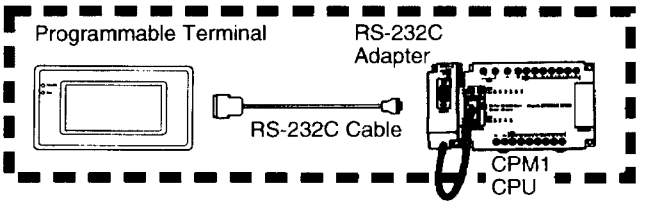


A Wide Variety of Built-in Features

- **External Input Interrupts**
  The 10-point CPM1 has up to 2 points while the 20 and 30-point CPM1s have up to 4 points available for external interrupt input. Input interrupt processing and counter processing are both available.
- **Quick-response Inputs**
  Inputs with a minimum input pulse width of 0.2 ms can be detected irrelevant of the cycle time.
- **Interval Timer Interrupts**
  The interval timer can be set from 0.5 to 319,968 ms. One-shot and scheduled interrupt modes are available.
- **High-speed Counter**
  The high-speed counter can be used in incrementing mode (5 kHz) or up/down mode (2.5 kHz). Using this counter together with the interrupts enables target value control and zone comparison control irrelevant of the cycle time.
- **Analog Volume Setting**
  Enables on-site adjustments of timer and counter settings by using two analog volume setting controls.
- **Input Time Constants**
  Input time constants of 1, 2, 4, 8, 16, 32, 64, or 128 ms can be selected to eliminate the effects of chattering and external noise for stable I/O operation.

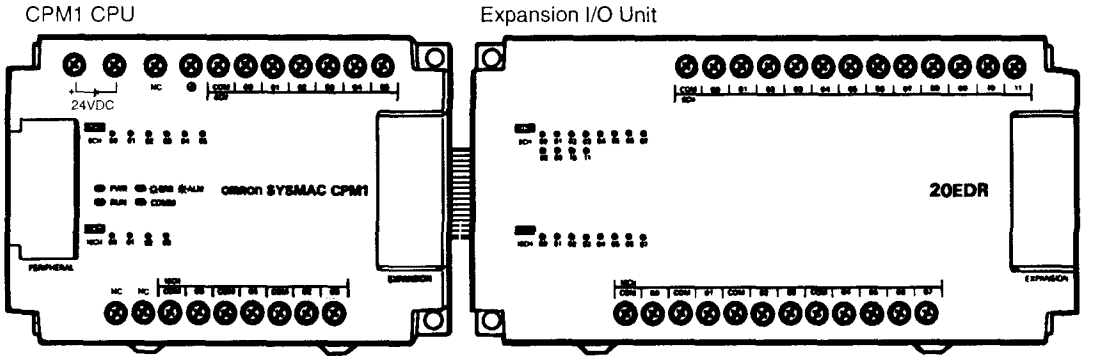
Easy Connection to a Programmable Terminal

High-speed communications can be achieved through the use of the NT Link between the CPM1 and Programmable Terminal.



Actual size

■ PLC Configuration



■ CPU

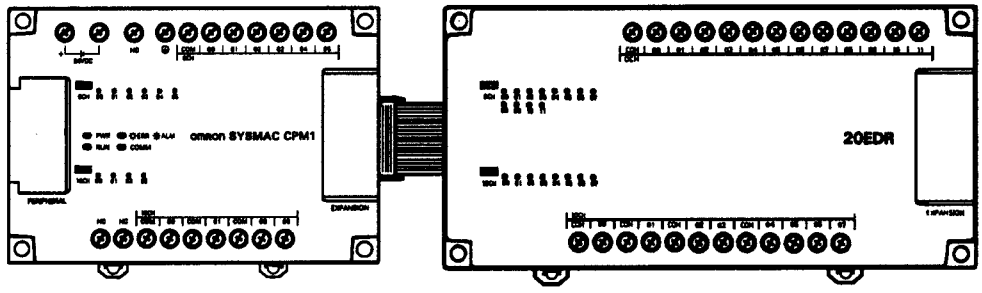
Type	Power supply	Output method	Input points	Output points	Model
10-point I/O	AC power supply	Relay output	6 points	4 points	CPM1-10CDR-A
	DC power supply				CPM1-10CDR-D
20-point I/O	AC power supply		12 points	8 points	CPM1-20CDR-A
	DC power supply				CPM1-20CDR-D
30-point I/O	AC power supply		18 points	12 points	CPM1-30CDR-A
	DC power supply				CPM1-30CDR-D

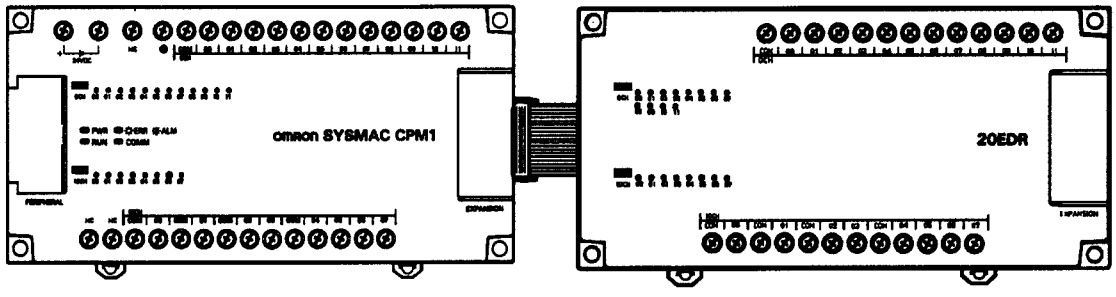
■ Expansion I/O Unit

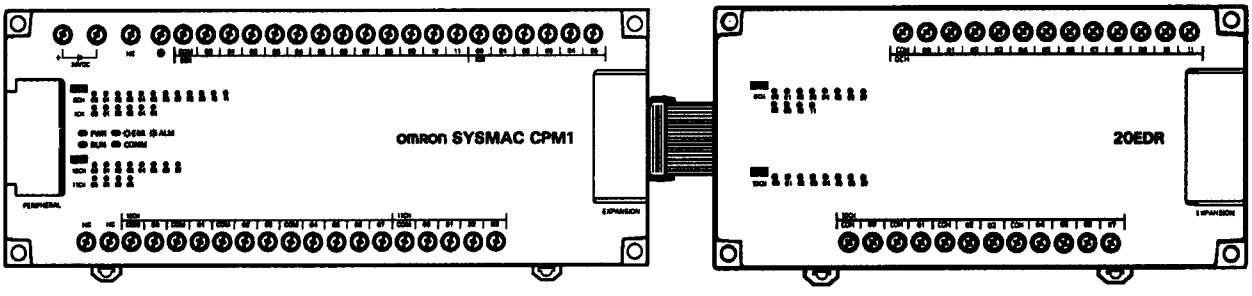
Type	Power supply	Output method	Input points	Output points	Model
20-point I/O	---	Relay output	12 points	8 points	CPM1-20EDR

■ I/O Points and Bits

The number of I/O points and the allocation of I/O bits for the CPM1 CPU and Expansion I/O Unit are given below.







Type	Power supply	Output type	Model	CPU only		With Expansion I/O Unit connected	
				Input	Output	Input	Output
10-point I/O	AC power supply	Relay output	CPM1-10CDR-A	6 points 00000 to 00005	4 points 01000 to 01003	18 points 00000 to 00005, 00100 to 00111	12 points 01000 to 01003, 01100 to 01107
	DC power supply		CPM1-10CDR-D				
20-point I/O	AC power supply		CPM1-20CDR-A	12 points 00000 to 00011	8 points 01000 to 01007	24 points 00000 to 00011, 00100 to 00111	16 points 01000 to 01007, 01100 to 01107
	DC power supply		CPM1-20CDR-D				
30-point I/O	AC power supply		CPM1-30CDR-A	18 points 00000 to 00011, 00100 to 00105	12 points 01000 to 01007, 01100 to 01103	30 points 00000 to 00011, 00100 to 00105, 00200 to 00211	20 points 01000 to 01007, 01100 to 01103, 01200 to 01207
	DC power supply		CPM1-30CDR-D				

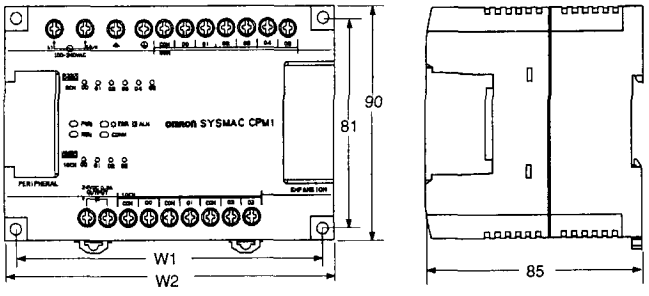
Specifications

■ General Specifications

Item		10-point I/O	20-point I/O	30-point I/O
Power supply voltage/ frequency	AC power supply	100 to 240 VAC, 50/60 Hz		
	DC power supply	24 VDC		
Operating voltage range	AC power supply	85 to 264 VAC		
	DC power supply	20.4 to 26.4 VDC		
Power consumption	AC power supply	60 VAC max.		
	DC power supply	20 W max.		
Inrush current		60 A max.		
External power supply (AC only)	Power supply voltage	24 VDC		
	Power supply output capacity	300 mA		
Insulation resistance		20 MΩ min. at 500 VDC between the AC terminals and the protective earth terminal.		
Dielectric strength		*2,300 VAC at 50/60 Hz for one minute with a leakage current of 10 mA max.* between all the external AC terminals and the protective earth terminal.		
Noise resistance		1,500 V (peak to peak) with a pulse width of 0.1 to 1 μs, and 1-ns rise time pulse (tested with a noise simulator)		
Vibration resistance		10 to 57 Hz with an amplitude of 0.075 mm, and 57 to 150 Hz with an acceleration of 9.8 m/s^2 (1 G) in the X, Y, and Z directions for 80 minutes each (i.e. swept for 8 minutes, 10 times).		
Shock resistance		197 m/s^2 (20 G) in the X, Y and Z directions 3 times each.		
Ambient temperature (operating)		0° to 55°C		
Ambient humidity (operating)		10% to 90% (no condensation)		
Ambient environment (operating)		With no corrosive gas		
Ambient temperature (storage)		*–20° to 75°C*		
Terminal screw size		M3		
Power supply holding time		10 ms min. for AC models, and 2 ms min. for DC models		
Weight		AC model: 600 g max. DC model: 500 g max.	AC model: 800 g max. DC model: 700 g max.	AC model: 900 g max. DC model: 800 g max.

■ Dimensions

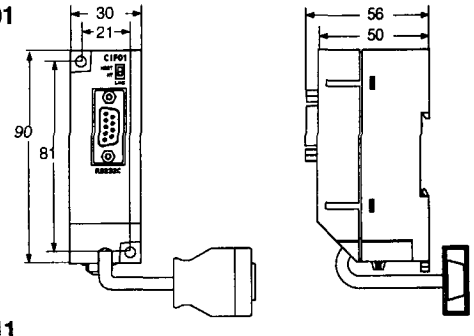
CPM1-□0CDR-□/CPM1-20EDR



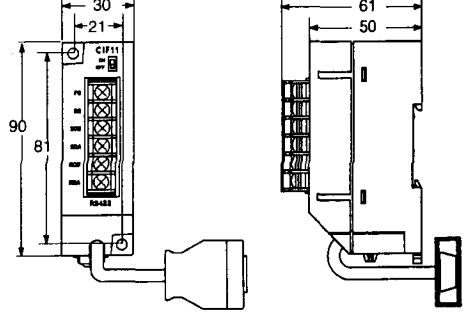
Width	CPM1-10CDR-□	CPM1-20CDR-□	CPM1-30CDR-□	CPM1-20EDR
W1	121	171	221	171
W2	130	180	230	180

Note: *All dimensions are in millimeters.*

CPM1-CIF01



CPM1-CIF11



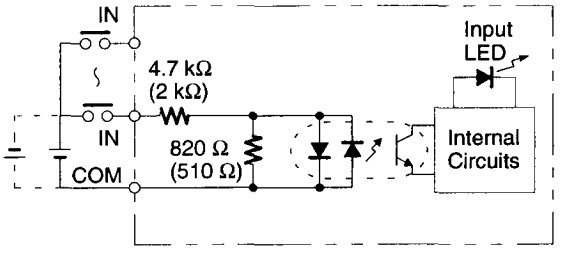
■ Performance Specifications

Item		10-point I/O	20-point I/O	30-point I/O
Control method		Stored program method		
I/O control method		Combination of the cyclic scan and immediate refresh processing methods.		
Programming language		Ladder diagram		
Instruction word		1 step per instruction, 1 to 5 words per instruction		
Types of instructions	Basic instructions	14 types		
	Special instructions	77 types, 134 instructions		
Instruction execution time	Basic instructions	0.72 to 16.2 μs		
	Special instructions	MOV instruction = 16.3 μs		
Program capacity		2,048 words		
Maximum I/O points	CPU only	10 points (6 input/4 output points)	20 points (12 input/8 output points)	30 points (18 input/12 output points)
	With Expansion I/O Unit	30 points (18 input/12 output points)	40 points (24 input/16 output points)	50 points (30 input/20 output points)
Input bits		00000 to 00915 (Bits not used as I/O bits can be used as work bits.)		
Output bits		01000 to 01915 (Bits not used as I/O bits can be used as work bits.)		
Work bits (IR Area)		640: IR 20000 to IR 23915 (IR 200 to IR 239)		
Special bits (SR Area)		256: SR 24000 to SR 25507 (SR 240 to SR 255)		
Temporary bits (TR Area)		8: TR 0 to TR 7		
Holding bits (HR Area)		320: HR 0000 to HR 1915 (HR 00 to HR 19)		
Auxiliary bits (AR Area)		256: AR 0000 to AR 1515 (AR 00 to AR 15)		
Link bits (LR Area)		256: LR 0000 to LR 1515 (LR 00 to LR 15)		
Timers/Counters		128: TIM/CNT 000 to 127 100-ms timer: TIM 000 to TIM 127 10-ms timer: TIM 000 to TIM 127 Decremental counter, reversible counter		
Data memory	Read/Write	1,024 words (DM 0000 to DM 1023)		
	Read only	512 words (DM 6144 to DM 6655)		
Interrupt processing: External interrupt		2 points (Response time of 0.3 ms max.)	4 points (Response time of 0.3 ms max.)	
Memory protection		Maintains the contents of the HR, AR, Counter and Data Memory Areas.		
Memory backup		Flash memory: User program, data memory (Read only) (Non-battery powered storage) Super capacitor: Data memory (Read/Write), holding bits, auxiliary memory bits, counter (20-day storage at an ambient temperature of 25°C)		
Self-diagnostic function		CPU error (watchdog timer), memory errors, I/O bus errors		
Program check		Program checks without an END instruction (constantly checked during operation)		
High-speed counter		1 point: Single phase at 5 kHz or two-phase at 2.5 kHz (linear counting method) Incremental mode: 0 to 65535 (16-bit) Decremental mode: –32767 to 32767 (16-bit)		
Quick-response inputs		Together with the external interrupt input (minimum pulse width of 0.2 ms)		
Input time constant		Can be set at 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms, or 128 ms.		
Analog volume settings		2 points: (0 to 200)		

■ I/O Specifications

Input Circuit

CPU

Item	Specifications	Circuit
Input voltage	24 VDC $^{+10\%}/_{-15\%}$	
Input impedance	IN0000 to IN0002: 2 kΩ Others: 4.7 kΩ	
Input current (typical)	IN0000 to IN0002: 12 mA Others: 5 mA	
ON voltage	14.4 VDC min.	
OFF voltage	5.0 VDC max.	
ON delay (see note 1)	8 ms max.	
OFF delay (see note 1)	8 ms max.	

Note Figures in parentheses are for IN00000 to IN00002.

Note: 1. The actual ON/OFF delay includes an input constant of 1, 2, 4, 8, 16, 32, 64, or 128 ms (default: 8 ms).

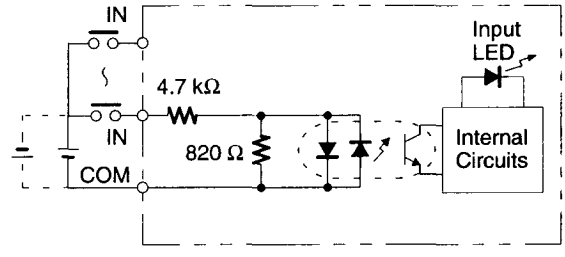
2. The delays for IN0000 to IN0002 are as follows when used for the high-speed counter.

Input	Increment mode	Differential phase mode
IN0000 (A-phase)	5 kHz	2.5 kHz
IN0001 (B-phase)	Normal input	
IN0002 (Z-phase)	ON: 100 μs max. OFF: 500 μs max.	

3. The delays for IN0003 to IN0006 are as follows when used for the high-speed counter.

Delay	0.3 ms max. (From the time of input ON until the interrupt subroutine is executed.)

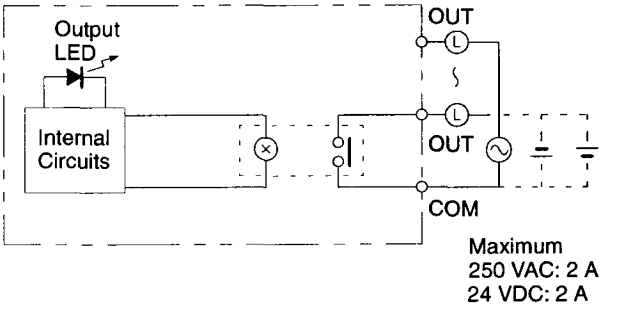
Expansion I/O Unit

Item	Specifications	Circuit
Input voltage	24 VDC, $^{+10\%}/_{-15\%}$	
Input impedance	4.7 kΩ	
Input current (typical)	5 mA	
ON voltage	14.4 VDC min.	
OFF voltage	5.0 VDC max.	
ON delay	8 ms max. (see note)	
OFF delay	8 ms max. (see note)	

Note: The actual ON/OFF delay includes an input constant of 1, 2, 4, 8, 16, 32, 64, or 128 ms (default: 8 ms).

Output Circuit

Relay Output (CPU and Expansion I/O Unit)

Item			Specifications	Circuit
Maximum switching capacity			250 VAC/2 A (cos ϕ =1) 24 VDC/2 A (4 A/common)	
Minimum switching capacity			5 VDC, 10 mA	
Applicable relays			OMRON G6R-1A	
Relay service life	Electrical	Resistance load	300,000 times	
		Inductive load	100,000 times	
	Mechanical		20,000,000 times	
ON delay			15 ms max.	
OFF delay			15 ms max.	

■ Communications Adapter Specifications

General Specifications

Item	Specifications	
	RS-232C Adapter	RS-422 Adapter
Functions	Level conversion between the CMOS level (CPU side) and the RS-232C (peripheral device side)	Level conversion between the CMOS level (CPU side) and the RS-422 (peripheral device side)
Insulation	The RS-232C (peripheral device side) is insulated by a DC/DC converter and photocoupler.	
Power supply	Power is supplied by the CPU.	
Power consumption	0.3 A max.	
Transmission speed	38.4 Kbits/s max.	
Vibration resistance	10 to 57 Hz with an amplitude of 0.075 mm, and 57 to 150 Hz with an acceleration of 9.8 m/s^2 (1 G) in the X, Y and Z directions for 80 minutes each in accordance (i.e. swept for 8 minutes, 10 times).	
Shock resistance	147 m/s^2 (15 G) in the X, Y and Z directions 3 times each.	
Ambient temperature (operating)	0° to 55°C	
Ambient humidity (operating)	10% to 90% (with no condensation)	
Ambient environment (operating)	With no corrosive gas	
Ambient temperature (storage)	–20° to 75°C	
Weight	200 g max.	

Bit Allocation

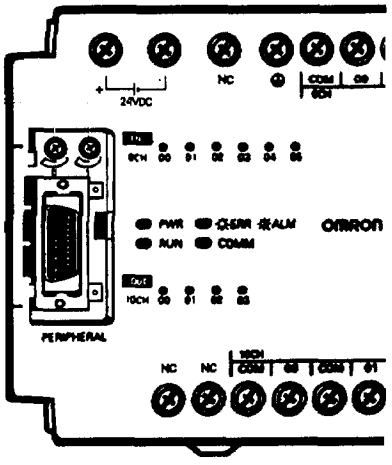
Name		No. of points	Word no.	Bit no.	Function
Input bits		160 points (10 words)	000 to 009	00000 to 00915	These bits can be used as an external I/O terminal. Bit numbers not used as I/O words may be used as work bits.
Output bits		160 points (10 words)	010 to 109	01000 to 01915	
Work bits (IR)		512 points (32 words)	IR 200 to IR 231	IR 20000 to IR 23115	These bits can be used for any purpose in a program.
Special auxiliary bits (SR)		384 points (24 words)	SR 232 to SR 255	SR 23200 to SR 25507	These bits are provided for specific functions.
Temporary memory bits (TR)		8 points	TR 0 to TR 7		These bits temporarily stores the ON/OFF status at circuit branch points.
Holding bits (HR)		320 points (20 words)	HR 00 to HR 19	HR 0000 to HR 1915	These bits can be used for any purpose in a program, and can even be used to store ON/OFF status in the event of a power interruption.
Auxiliary bits (AR)		256 points (16 words)	AR 00 to AR 15	AR 0000 to AR 1515	These bits are provided for specific functions, and can even be used to store ON/OFF status in the event of a power interruption.
Link bits (LR)		256 points (16 words)	LR 00 to LR 15	LR 0000 to LR 1515	These bits are used for 1:1 link data I/O. These can also be used as work bits.
Timer/Counter (TIM/CNT)		128 points	TIM/CNT 000 to TIM/CNT 127		These are for the timer and the counter. The same number is used for both.
Data memory (DM)	Read/Write enable	1,002 words	DM 0000 to DM 0999, DM 1022 to DM 1023		Data memory uses word units (16-bit structure) to store data in the event of a power interruption. When DM 6144 to DM 6599 and DM 6600 to DM 6655 are serving as regular data memory (DM), then programs cannot write to these blocks as long as no error history is stored in DM 1000 to DM 1021. (This can be set from peripheral devices.)
	Error history storage area	22 words	DM 1000 to DM 1021		
	Read only enable	426 words	DM 6144 to DM 6599		
	PLC setup area	56 words	DM 6600 to DM 6655		

Analog Volume Setting

The CPM1 PLC contains two analog volume setting controls that can be used for a broad range of analog timer and counter settings. Turning the volume control stores values of 0 to 200 (BCD data) in the SR area.

Adjust the volume control with a Phillips-head screwdriver.

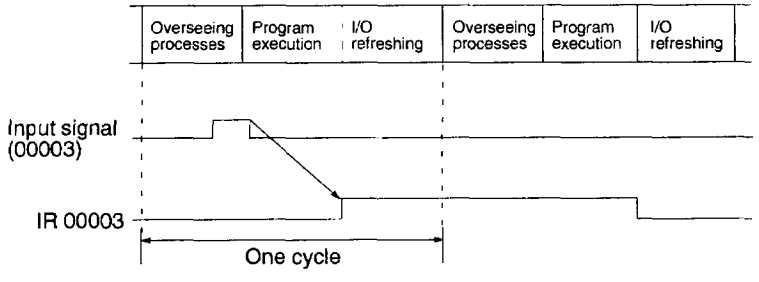
Analog volume control 0
Analog volume control 1



Analog volume setting	Storage area	Setting value (BCD)
Analog volume setting 0	SR 250	0000 to 0200
Analog volume setting 1	SR 251	

Quick-response Inputs

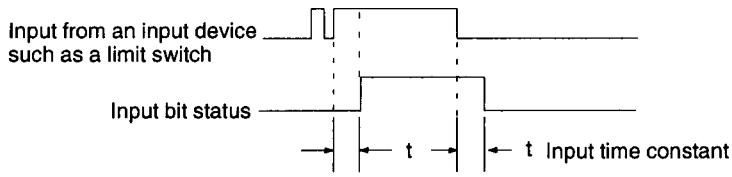
There are two quick-response inputs for the CPM1 10-point I/O PLC and four for the 20 and 30-point I/O PLC (shared with the interrupt inputs). Since an internal buffer is provided, the quick-response input function can even detect signals modified within one cycle.



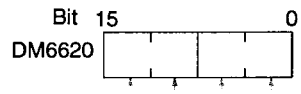
CPU	Input no.	Minimum input pulse width
10-point I/O CPU	00003 to 00004	0.2 ms
20-point, 30-point I/O CPU	00003 to 00006	

Input Time Constants

Input time constants of 1, 2, 4, 8, 16, 32, 64, or 128 ms can be selected for CPM1 external inputs. Increasing the input time constant reduces chattering and external noise.



■ Input Time Constants for IR 000

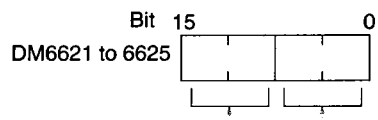


Time constant for IR 00007 to IR 00011 (1 digit BCD; see below.)
Time constant for IR 00005 to IR 00006 (1 digit BCD; see below.)
Time constant for IR 00003 to IR 00004 (1 digit BCD; see below.)
Time constant for IR 00000 to IR 00002 (1 digit BCD; see below.)

Default: 8 ms for each.

■ Input Time Constants for IR 001 to IR 009

DM 6621 : IR 001 and IR 002
DM 6622 : IR 003 and IR 004
DM 6623 : IR 005 and IR 006
DM 6624 : IR 007 and IR 008
DM 6625 : IR 009



Time constant for IR 002, IR 004, IR 006, and IR 008
Time constant for IR 001, IR 003, IR 005, IR 007, and IR 009

Default: 8 ms for each.

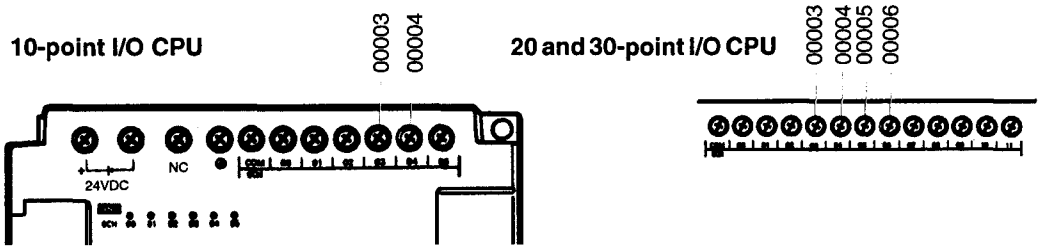
The nine possible settings for the input time constant are shown below. Set only the rightmost digit for IR 000.

0: 8 ms 1: 1 ms 2: 2 ms 3: 4 ms 4: 8 ms 5: 16 ms 6: 32 ms 7: 64 ms 8: 128 ms

The CPM1's I/O response time is the input time constant (1 ms to 128 ms; default is 8 ms) + the cycle time.

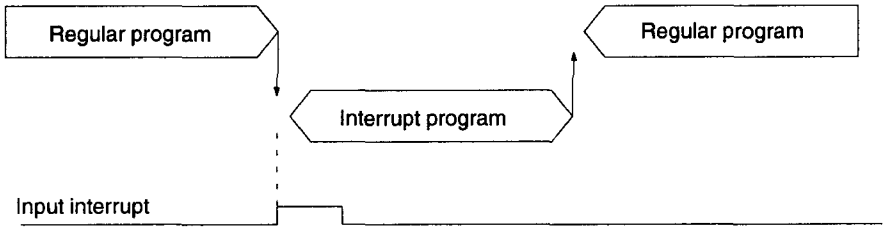
Input Interrupts

There are two input interrupts in the CPM1 10-point I/O CPU and four in the 20 and 30-point I/O CPU. Input interrupts are available in two modes.



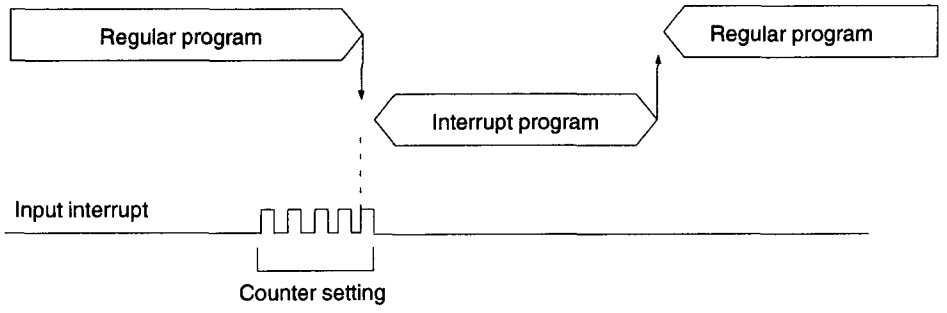
Input Interrupt Mode

If an input interrupt occurs, the regular program shuts down irrelevant of the cycle time, and the interrupt processing program is executed immediately.



Counter Mode

When external signals are counted at high speed, the regular program shuts down, and the interrupt processing program is executed at fixed counts. The count can be set between 0 and 65535.



CPU	Input no.	Interrupt no.	Response time	
			Input interrupt mode	Counter mode
10-point I/O CPU	*00003*	*00*	*0.3 ms max. (Time until the interrupt sub-routine triggers)*	*1 kHz*
	00004	01		
20-point I/O CPU 30-point I/O CPU	00003	00		
	00004	01		
	00005	02		
	00006	03		

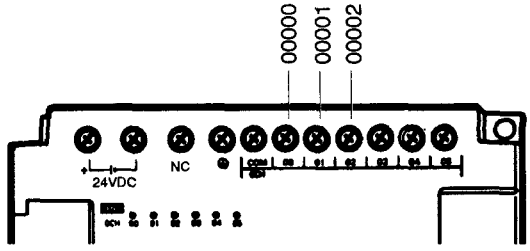
Interval Timer Interrupts

The CPM1 has one interval timer. The interval timer shuts down the regular program irrelevant of the point in the cycle once the time is up, and immediately executes an interrupt processing program. Interval timers are used in the following two modes.

Item	One-shot mode	Scheduled interrupt mode
Operation	An interrupt is executed only once when the time is up.	Interrupts are executed repeatedly at fixed periods.
Setting time	*0.5 ms to 319,968 ms (0.1-ms units)*	

High-speed Counter

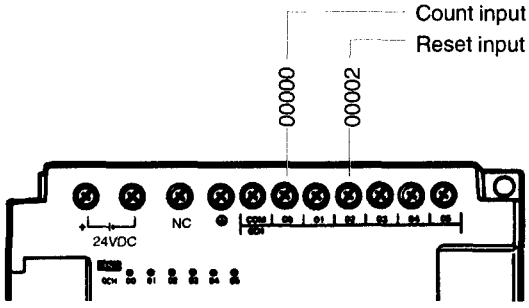
The CPM1 has a high-speed counter function that can be used in the incrementing and up/down mode. Using this function together with the input interrupts enables zone comparison control or target value control irrelevant of the cycle time.

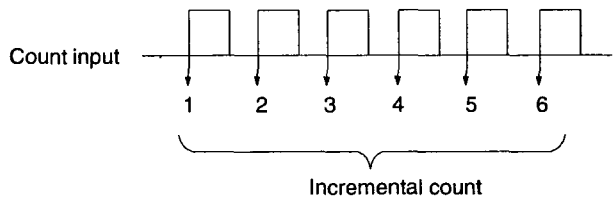


Item		Incrementing mode	Up/Down mode
Input no.	00000	Count input	A-phase input
	00001	---	B-phase input
	00002	Reset input	Z-phase input
Input method		Individual inputs	Phase-difference, 4× inputs
Count frequency		5.0 kHz	2.5 kHz
Count range		0 to 65535	–32767 to 32767
Control method	Target value control	16 target values and interrupt subroutine numbers can be registered.	
	Zone comparison control	8 sets of upper and lower limit values and interrupt subroutine numbers can be registered.	

■ Incremental Mode Operation

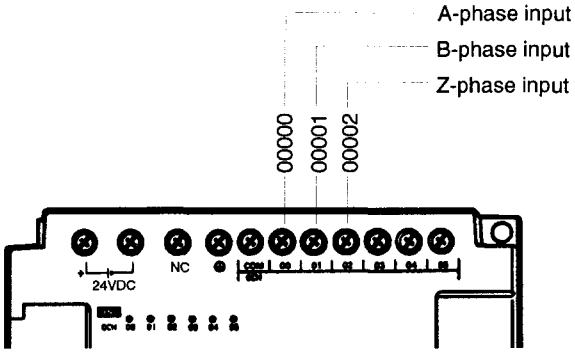
When one single-phase signal and a count reset signal are input, the single-phase signal is used to count incrementally. The count reset can be used for a software reset.

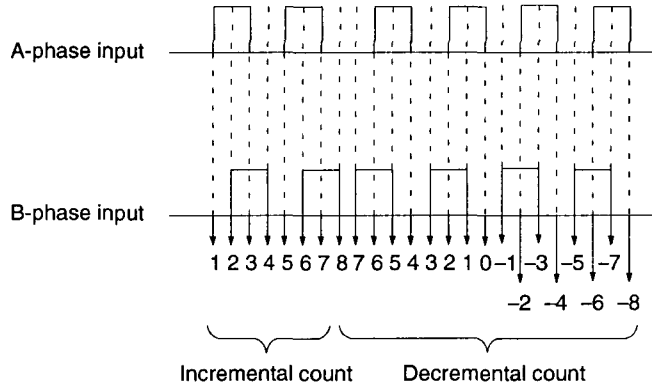




■ Adjustable Mode Operation

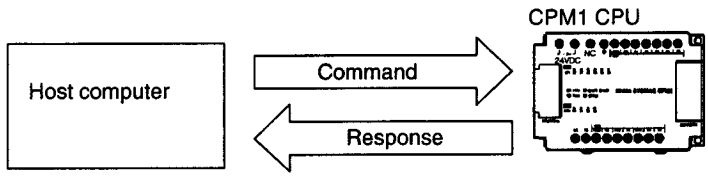
When a Z-phase signal and a two-phase (A-phase and B-phase) with a phase differential of at least a factor of 4 are input, the two-phase signal shift is used for incremental and decremental counts. The counter is reset by the Z-phase input or by a software reset.



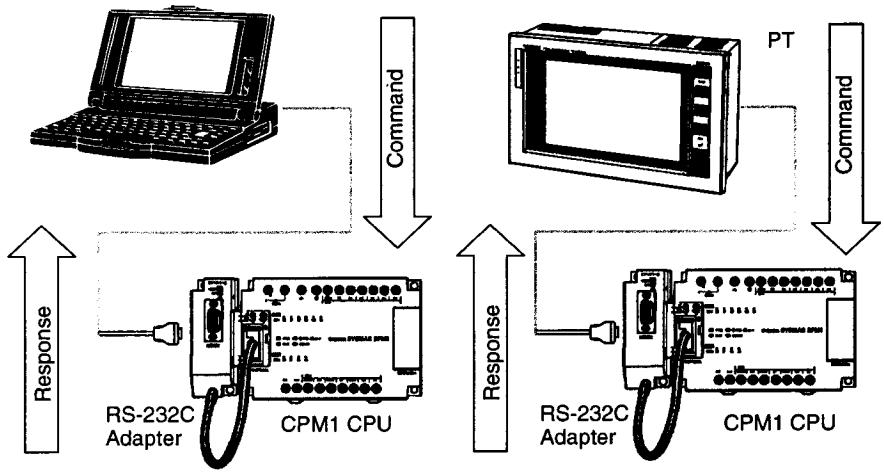


Host Link Communications

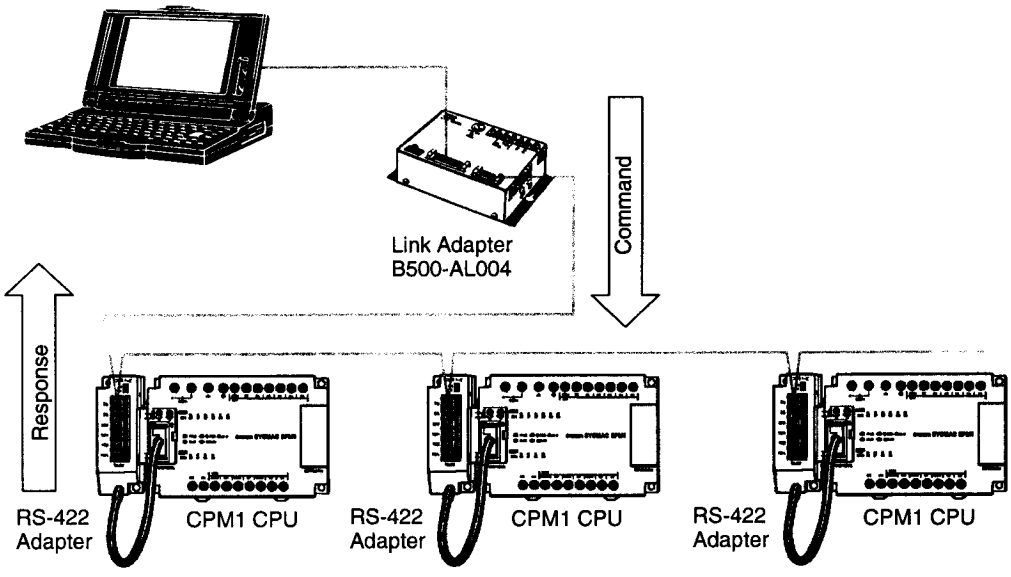
CPM1 host link communications consist of interactive procedures whereby a PLC returns a response to a command sent from the host computer. These communications allow the host computer to read and write in the PLC's I/O Areas and Data Memory Areas as well as in areas containing the status of various settings.



1:1 Host Link Communications



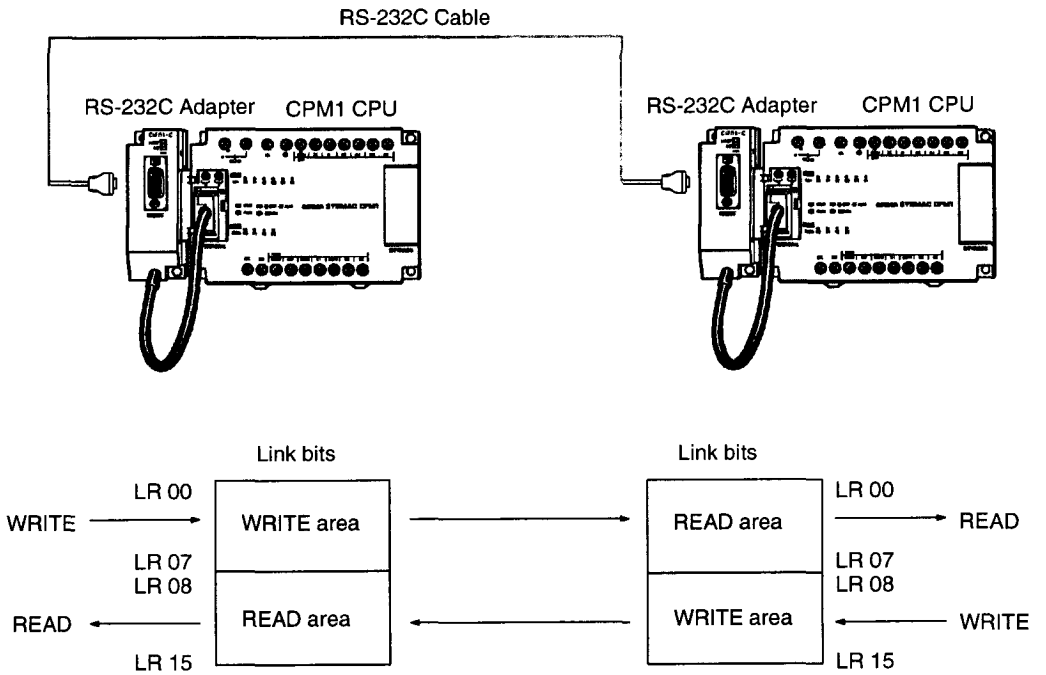
1:n Host Link Communications



1:1 Links

With a 1:1 link, two CPM1 PLCs or a CPM1 PLC and CQM1 or C200H□ PLC are connected 1:1 with one side as the Master and the other as the Slave to provide an I/O link of a maximum of 256 points (LR 0000 to LR 1515).

Example of a 1:1 Link between CPM1 PLCs

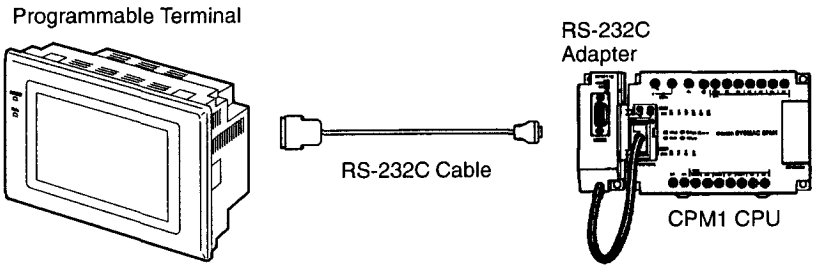


Limitations of the CPM1 1:1 Link

CPM1 I/O links are limited to 16 words (LR 00 to LR 15). Therefore, use these 16 words (LR 00 to LR 15) on the CQM1 or C200HS side when forming 1:1 links with a CQM1 or C200HS. LR 16 to LR 63 cannot be used to form 1:1 links with a CPM1.

NT Links

High-speed communications can be achieved by providing a direct access through the use of the NT Link between the CPM1 and Programmable Terminal.



Note: The NT Link can only be used when the *RS-232C Adapter (CPM1-CIF01) is connected.*

Programming Instructions

Summary of Programming Instructions

■ Function Code Chart

Table symbols	Details	Key operations for specifying programming instructions
○	Allocated to instruction keys on the Programming Console. These need not be specified with function codes.	---
Code	Special instructions specified with function codes.	FUN → Code → WRITE
★	Expansion instructions. The following operations are required in order to use these instructions.	(After sorting operations) FUN → Code → WRITE
*□	These can only be used on CPUs.	---

■ Differentiated Instructions

Differentiated instructions can sometimes be used for CPM1 special instructions. Instructions marked with (@) in the mnemonics can also be used as differentiated instructions. Here the input rise time (shift from OFF to ON) is used to execute the instruction in just one cycle.

To specify an instruction, press the NOT Key after the function code.

Example: Specifying the @MOV (21) instruction

FUN 2 1 NOT WRITE

■ Sequence Instructions

Sequence Input Instructions

Instruction	Mnemonic	Code	Function
LOAD	LD	○	Connects an NO condition to the left bus bar.
LOAD NOT	LD NOT	○	Connects an NC condition to the left bus bar.
AND	AND	○	Connects an NO condition in series with the previous condition.
AND NOT	AND NOT	○	Connects an NC condition in series with the previous condition.
OR	OR	○	Connects an NO condition in parallel with the previous condition.
OR NOT	OR NOT	○	Connects an NC condition in parallel with the previous condition.
AND LOAD	AND LD	○	Connects two instruction blocks in series.
OR LOAD	OR LD	○	Connects two instruction blocks in parallel.

Note: ○: Instruction keys allocated to the Programming Console.

Sequence Output Instructions

Instruction	Mnemonic	Code	Function
OUTPUT	OUT	○	Outputs the result of logic to a bit.
OUT NOT	OUT NOT	○	Reverses and outputs the result of logic to a bit.
SET	SET	○	Force sets (ON) a bit.
RESET	RSET	○	Force resets (OFF) a bit.
KEEP	KEEP	11	Maintains the status of the designated bit.
DIFFERENTIATE UP	DIFU	13	Turns ON a bit for one cycle when the execution condition goes from OFF to ON.
DIFFERENTIATE DOWN	DIFD	14	Turns ON a bit for one cycle when the execution condition goes from ON to OFF.

Note: ○: Instruction keys allocated to the Programming Console.

Sequence Control Instructions

Instruction	Mnemonic	Code	Function
NO OPERATION	NOP	00	---
END	END	01	Required at the end of the program.
INTERLOCK	IL	02	If the execution condition for IL(02) is OFF, all outputs are turned OFF and all timer PVs reset between IL(02) and the next ILC(03).
INTERLOCK CLEAR	ILC	03	ILC(03) indicates the end of an interlock (beginning at IL(02)).
JUMP	JMP	04	If the execution condition for JMP(04) is ON, all instructions between JMP(04) and JME(05) are treated as NOP(00).
JUMP END	JME	05	JME(05) indicates the end of a jump (beginning at JMP(04)).

Timer/Counter Instructions

Instruction	Mnemonic	Code	Function
TIMER	TIM	○	An ON-delay (decrementing) timer.
COUNTER	CNT	○	A decrementing counter.
REVERSIBLE COUNTER	CNTR	12	Increases or decreases PV by one.
HIGH-SPEED TIMER	TIMH	15	A high-speed, ON-delay (decrementing) timer.

Note: ○: Instruction keys allocated to the Programming Console.

Data Comparison Instructions

Instruction	Mnemonic	Code	Function
COMPARE	CMP	20	Compares two four-digit hexadecimal values.
DOUBLE COMPARE	CMPL	60	Compares two eight-digit hexadecimal values.
BLOCK COMPARE	(@)BCMP	68	Judges whether the value of a word is within 16 ranges (defined by lower and upper limits).
TABLE COMPARE	(@)TCMP	85	Compares the value of a word to 16 consecutive words.

■ Data Movement Instructions

Instruction	Mnemonic	Code	Function
MOVE	(@)MOV	21	Copies a constant or the content of a word to a word.
MOVE NOT	(@)MVN	22	Copies the complement of a constant or the content of a word to a word.
BLOCK TRANSFER	(@)XFER	70	Copies the content of a block of up to 1,000 consecutive words to a block of consecutive words.
BLOCK SET	(@)BSET	71	Copies the content of a word to a block of consecutive words.
DATA EXCHANGE	(@)XCHG	73	Exchanges the content of two words.
SINGLE WORD DISTRIBUTE	(@)DIST	80	Copies the content of a word to a word (whose address is determined by adding an offset to a word address).
DATA COLLECT	(@)COLL	81	Copies the content of a word (whose address is determined by adding an offset to a word address) to a word.
MOVE BIT	(@)MOVB	82	Copies the specified bit from one word to the specified bit of a word.
MOVE DIGIT	(@)MOVD	83	Copies the specified digits (4-bit units) from a word to the specified digits of a word.

■ Shift Instructions

Instruction	Mnemonic	Code	Function
SHIFT REGISTER	SFT	○/10	Copies the specified bit (0 or 1) into the rightmost bit of a shift register and shifts the other bits one bit to the left.
WORD SHIFT	(@)WSFT	16	Creates a multiple-word shift register that shifts data to the left in one-word units.
ASYNCHRONOUS SHIFT REGISTER	(@)ASFT	17	Creates a shift register that exchanges the contents of adjacent words when one is zero and the other is not.
ARITHMETIC SHIFT LEFT	(@)ASL	25	Shifts a 0 into bit 00 of the specified word and shifts the other bits one bit to the left.
ARITHMETIC SHIFT RIGHT	(@)ASR	26	Shifts a 0 into bit 15 of the specified word and shifts the other bits one bit to the right.
ROTATE LEFT	(@)ROL	27	Moves the content of CY into bit 00 of the specified word, shifts the other bits one bit to the left, and moves bit 15 to CY.
ROTATE RIGHT	(@)ROR	28	Moves the content of CY into bit 15 of the specified word, shifts the other bits one bit to the right, and moves bit 00 to CY.
ONE DIGIT SHIFT LEFT	(@)SLD	74	Shifts a 0 into the rightmost digit (4-bit unit) of the shift register and shifts the other digits one digit to the left.
ONE DIGIT SHIFT RIGHT	(@)SRD	75	Shifts a 0 into the leftmost digit (4-bit unit) of the shift register and shifts the other digits one digit to the right.
REVERSIBLE SHIFT REGISTER	(@)SFTR	84	Creates a single or multiple-word shift register that can shift data to the left or right.

Note: ○: Instruction keys allocated to the Programming Console.

■ Increment/Decrement Instructions

Instruction	Mnemonic	Code	Function
INCREMENT	(@)INC	38	Increments the BCD content of the specified word by 1.
DECREMENT	(@)DEC	39	Decrements the BCD content of the specified word by 1.

■ BCD/Binary Calculation Instructions

Instruction	Mnemonic	Code	Function
BCD ADD	(@)ADD	30	Adds the content of a word (or a constant).
BCD SUBTRACT	(@)SUB	31	Subtracts the content of a word (or constant) and CY from the content of a word (or constant).
BCD MULTIPLY	(@)MUL	32	Multiplies the contents of two words (or constants).
BCD DIVIDE	(@)DIV	33	Divides the content of a word (or constant) by the content of a word (or constant).
BINARY ADD	(@)ADB	50	Adds the contents of two words (or constants) and CY.
BINARY SUBTRACT	(@)SBB	51	Subtracts the content of a word (or constant) and CY from the content of a word (or constant).
BINARY MULTIPLY	(@)MLB	52	Multiplies the contents of two words (or constants).
BINARY DIVIDE	(@)DVB	53	Divides the content of a word (or constant) by the content of a word and obtains the result and remainder.
DOUBLE BCD ADD	(@)ADDL	54	Add the 8-digit BCD contents of two pairs of words (or constants) and CY.
DOUBLE BCD SUBTRACT	(@)SUBL	55	Subtracts the 8-digit BCD contents of a pair of words (or constants) and CY from the 8-digit BCD contents of a pair of words (or constants).
DOUBLE BCD MULTIPLY	(@)MULL	56	Multiplies the 8-digit BCD contents of two pairs of words (or constants).
DOUBLE BCD DIVIDE	(@)DIVL	57	Divides the 8-digit BCD contents of a pair of words (or constants) by the 8-digit BCD contents of a pair of words (or constants).

■ Data Conversion Instructions

Instruction	Mnemonic	Code	Function
BCD TO BINARY	(@)BIN	23	Converts 4-digit BCD data to 4-digit binary data.
BINARY TO BCD	(@)BCD	24	Converts 4-digit binary data to 4-digit BCD data.
4 TO 16 DECODER	(@)MLPX	76	Takes the hexadecimal value of the specified digit(s) in a word and turns ON the corresponding bit in a word(s).
16 TO 4 DECODER	(@)DMPX	77	Identifies the highest ON bit in the specified word(s) and moves the hexadecimal value(s) corresponding to its location to the specified digit(s) in a word.
ASCII CODE CONVERT	(@)ASC	86	Converts the designated digit(s) of a word into the equivalent 8-bit ASCII code.

■ Logic Instructions

Instruction	Mnemonic	Code	Function
COMPLEMENT	(@)COM	29	Turns OFF all ON bits and turns ON all OFF bits in the specified word.
LOGICAL AND	(@)ANDW	34	Logically ANDs the corresponding bits of two words (or constants).
LOGICAL OR	(@)ORW	35	Logically ORs the corresponding bits of two words (or constants).
EXCLUSIVE OR	(@)XORW	36	Exclusively ORs the corresponding bits of two words (or constants).
EXCLUSIVE NOR	(@)XNRW	37	Exclusively NORs the corresponding bits of two words (or constants).

■ Special Calculation Instructions

Instruction	Mnemonic	Code	Function
BIT COUNTER	(@)BCNT	67	Counts the total number of bits that are ON in the specified block of words.

■ Subroutine Instructions

Instruction	Mnemonic	Code	Function
SUBROUTINE ENTER	(@)SBS	91	Executes a subroutine in the main program.
SUBROUTINE ENTRY	SBN	92	Marks the beginning of a subroutine program.
SUBROUTINE RETURN	RET	93	Marks the end of a subroutine program.
MACRO	MCRO	99	Calls and executes the specified subroutine, substituting the specified input and output words for the input and output words in the subroutine.

■ Interrupt Control Instructions

Instruction	Mnemonic	Code	Function
INTERVAL TIMER	(@)STIM	69	Controls interval timers used to perform scheduled interrupts.
INTERRUPT CONTROL	(@)INT	89	Performs interrupt control, such as masking and unmasking the interrupt bits for I/O interrupts.

■ Step Instructions

Instruction	Mnemonic	Code	Function
STEP DEFINE	STEP	08	Defines the start of a new step and resets the previous step when used with a control bit. Defines the end of step execution when used without a control bit.
STEP START	SNXT	09	Starts the execution of the step when used with a control bit.

■ Peripheral Device Control Instruction

I/O Unit Instructions

Instruction	Mnemonic	Code	Function
7-SEGMENT DECODER	(@)SDEC	78	Converts the designated digit(s) of a word into an 8-bit, 7-segment display code.
I/O REFRESH	(@)IORF	97	Refreshes the specified I/O word.

Display Instructions

Instruction	Mnemonic	Code	Function
MESSAGE	(@)MSG	46	Reads up to 8 words of ASCII code (16 characters) from memory and displays the message on the Programming Console or other Peripheral Device.

High-speed Counter Control Instructions

Instruction	Mnemonic	Code	Function
MODE CONTROL	(@)INI	61	Starts and stops counter operation, compares and changes counter PVs, and stops pulse output.
PV READ	(@)PRV	62	Reads counter PVs and status data.
COMPARE TABLE LOAD	(@)CTBL	63	Compares counter PVs and generates a direct table or starts operation.

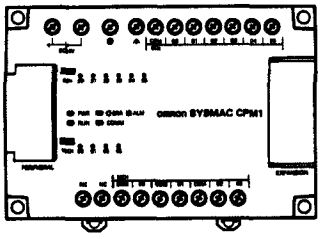
■ Damage Diagnosis Instructions

Instruction	Mnemonic	Code	Function
FAILURE ALARM	(@)FAL	06	Generates a non-fatal error when executed. The Error/Alarm indicator flashes and the CPU continues operating.
SEVERE FAILURE ALARM	FALS	07	Generates a fatal error when executed. The Error/Alarm indicator lights and the CPU stops operating.

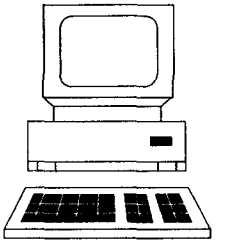
■ Special System Instructions

Instruction	Mnemonic	Code	Function
SET CARRY	(@)STC	40	Sets Carry Flag 25504 to 1.
CLEAR CARRY	(@)CLC	41	Sets Carry Flag 25504 to 0.

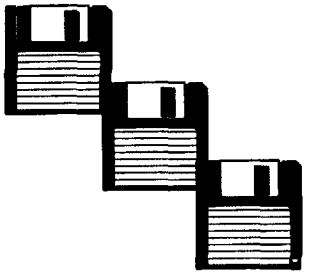
CPM1 CPU



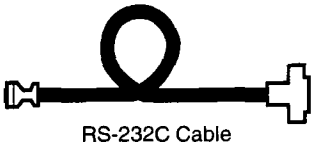
IBM PC/AT or compatible



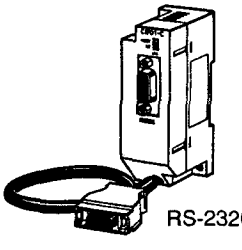
SYSWIN,
SYSMAC Support Software



CQM1-CIF02

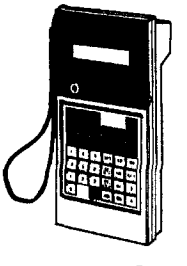


RS-232C Cable

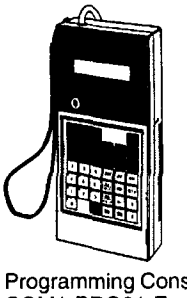


RS-232C Adapter

C200HS-CN222/CN422



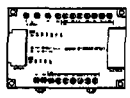
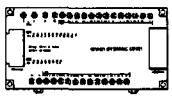
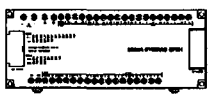
Programming Console
C200H-PRO27-E



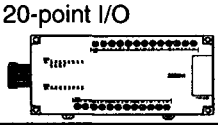
Programming Console
CQM1-PRO01-E

Standard Models

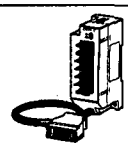
■ CPU

Name	Power supply	Output method	Input points	Output points	Model
10-point I/O 	AC power supply	Relay output	6 points	4 points	CPM1-10CDR-A
	DC power supply				CPM1-10CDR-D
20-point I/O 	AC power supply		12 points	8 points	CPM1-20CDR-A
	DC power supply				CPM1-20CDR-D
30-point I/O 	AC power supply		18 points	12 points	CPM1-30CDR-A
	DC power supply				CPM1-30CDR-D

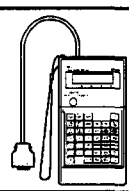
■ Expansion I/O Unit

Name	Power supply	Output method	Input points	Output points	Model
20-point I/O 	---	Relay output	12 points	8 points	CPM1-20EDR

■ RS-232C Adapter, RS-422 Adapter, Connecting Cable, Link Adapter

Name	Function	Model
RS-232C Adapter 	Converts peripheral port levels.	CPM1-CIF01
RS-422 Adapter 		CPM1-CIF11
Connecting Cable	3.3-m cable used to connect IBM PC/AT or compatible personal computers.	CQM1-CIF02
Link Adapter	Converts RS-232C and RS-422 levels.	3G2A9-AL004-E

■ Programming Console

Name	Function	Model
Programming Console 	With a 2-m cable	CQM1-PRO01-E
	---	C200H-PRO27-E
	2-m Connecting Cable for C200H-PRO27-E	C200HS-CN222
	4-m Connecting Cable for C200H-PRO01-E	C200HS-CN422

■ Programming Software

Name	Operating system	Operating environment	Model
SYSMAC Support Software	MS-DOS Ver. 5.0 or later	Used in IBM PC/AT or compatible personal computers (i386/i486/Pentium)	C500-ZL3AT1-E
SYSWIN	MS-WINDOWS Ver. 3.1 or later		SYSWIN-CPM1-V3.X

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